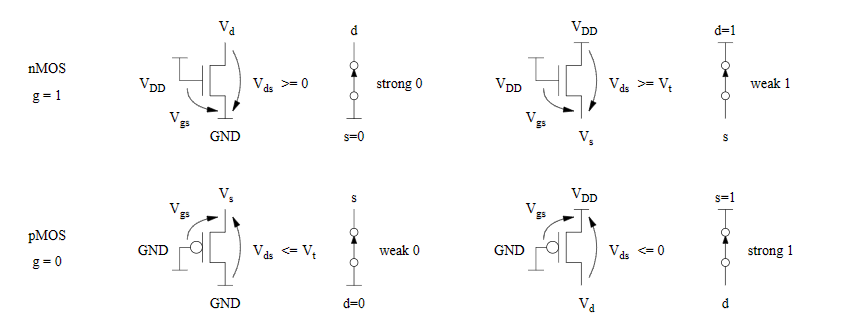
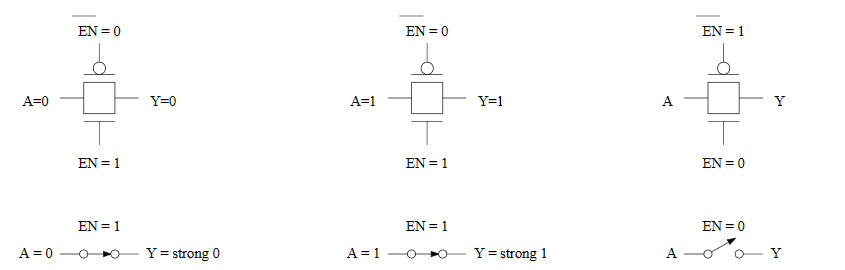
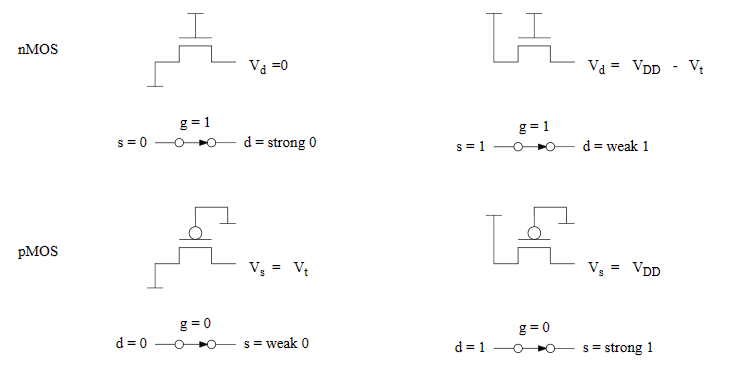
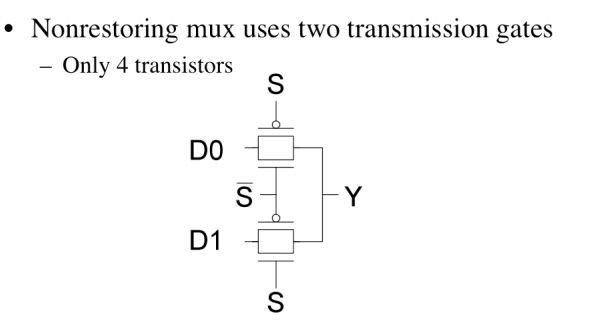
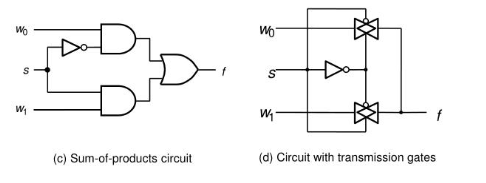
**Transmission Gate**

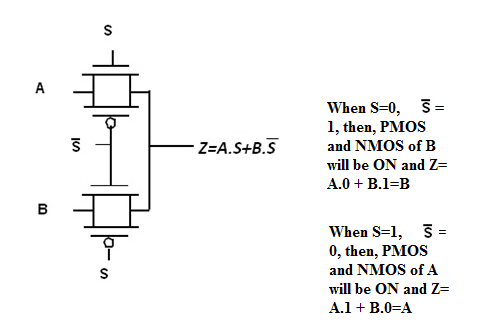




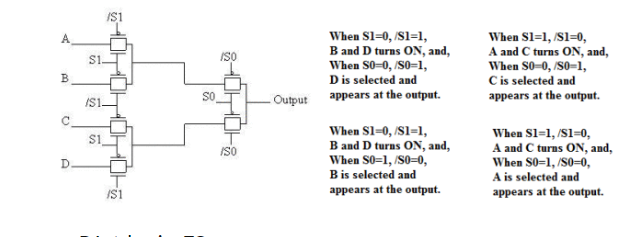
**2:1 mux**



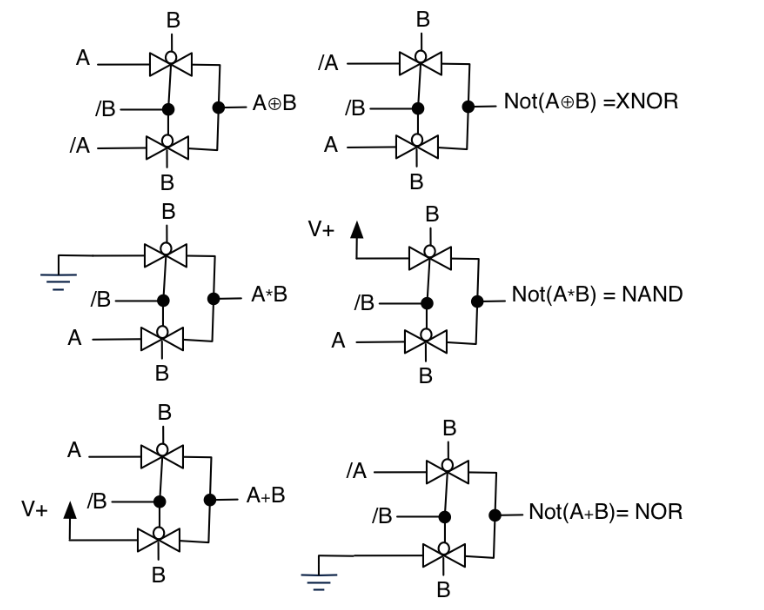




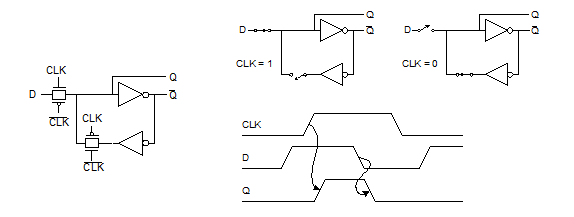
**4:1 Mux**



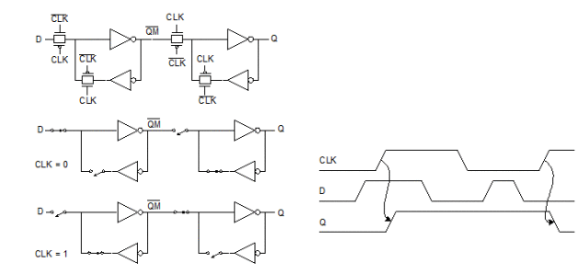
**Transmission as a logic gates**

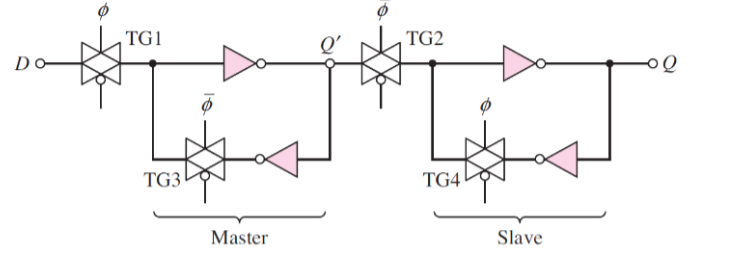


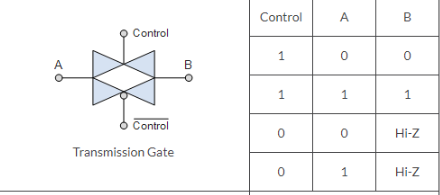
**D Latch**

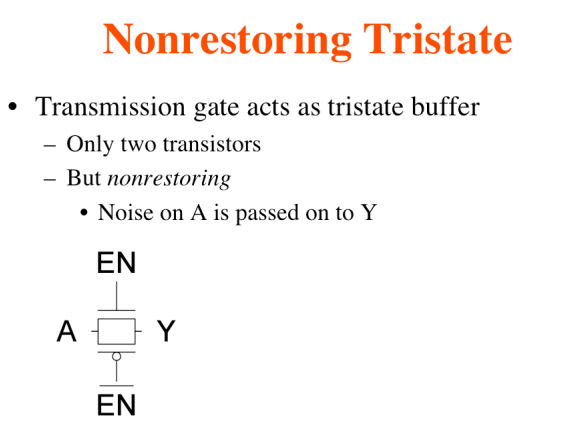


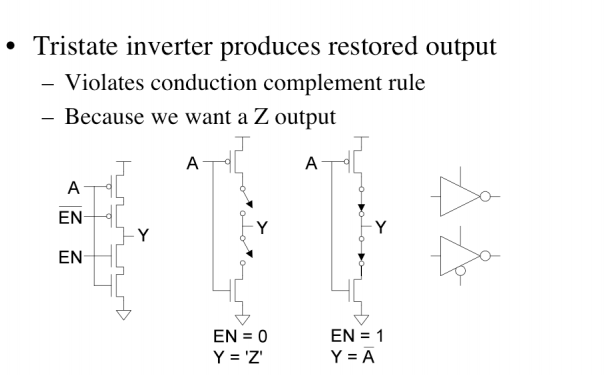
D-Flipflop

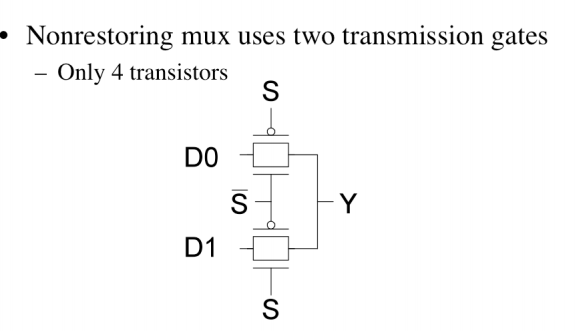












Restoring gates mux

